

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 5

Application Number 09/592,106
Filing Date 06/12/2000
First Named Inventor Stephen Melvin
Art Unit 2154
Examiner Name Larry D. Donaghue
Attorney Docket Number P3813

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5600837 A *	02-04-1997	Artieri, Alain	
		US- 5461722 A *	10-24-1995	Goto, Tatuhiro	
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		US- 5748468 A *	05-05-1998	Notenboom et al.	
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		US- 5867725 A *	02-02-1999	Fung et al.	
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**INFORMATION DISCLOSURE
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Sheet 2 of 5**Complete if Known**

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First Named Inventor	Stephen Melvin
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		Number-Kind Code ² (if known)			
S S S S S S S S S S S S S S		US- 6535905 B1 *	03-18-2003	Kalafatis et al.	
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		US- 5987492 A *	11-16-1999	Yue, Kelvin	
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		US- 6052708 A *	04-18-2000	Flynn et al.	
		US- 6212544 B1 *	04-03-2001	Borkenhagen et al.	
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First Named Inventor Stephen Melvin

Art Unit 2154

Examiner Name

Larry D. Donaghue Technology Center 2100

Attorney Docket Number P3813

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JS		* FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
JS		* YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of California Santa Barbara dissertation, December 1995, Santa Barbara, US	
JS		* STEERE et al., "A Feedback - Driven Proportion Allocator for Real-Rate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp.145-158, USENIX Association	
JS		* YAMAMOTO et al., "Increasing Superscalar Performance Through Multistreaming", 1995	
JS		* TULLSEN et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22nd Annual International Symposium on Computer Architecture, June 1995, Santa Margherita Ligure, Italy	
JS		* YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp 42-53, IEEE	
JS		* KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 Mhz", August 1998	
JS		* YAMAMOTO ET AL., Performance Estimation of Multistreamed, Superscalar Processors, IEEE. 1994, pp 195-204, Hawaii, US	
JS		* NEMIROVSKY et al., "Quantitative Study of Data Caches on a Multistreamed Architecture", Workshop on Multithreaded Execution Architecture and Compilation, January 1998	
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		Application Number	09/592,106		
		Filing Date	06/12/2000		
		First Named Inventor	Stephen Melvin		
		Art Unit	2154		
		Examiner Name	Larry D. Donaghy		
Sheet	4	of	5	Attorney Docket Number	P3813

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NON PATENT LITERATURE DOCUMENTS			
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		* The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan Kaufmann, San Francisco	
		* MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
		* POTEL, M.J., Real-Time Playback in Animation Systems, Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp. 72-77, San Jose, CA	
		* ARM Architecture Reference Manual, 1996, pp. 3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall	
		* ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at : http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS)	
		* MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp. 10-66, 10-67 and 10-71, Motorola, Inc.	
		* DIFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, pp.40-63, Vol. 12, No. 2	
		* KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp 7-106 and 7-107, Prentice Hall, New Jersey	
		* DIFENDORFF, KEITH et al., AltiVec Extension to PowerPC Accelerates Media Processing, March - April 2000, pp. 85-95, IEEE Micro, Vol. 20, No. 2	
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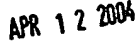
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2154

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* DONALSON ET AL., "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance", 26th Hawaii Conference on Systems Sciences, 1993, pp 448-456, vol. 1

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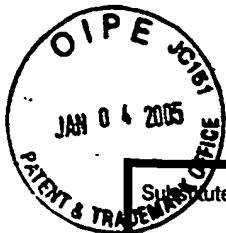
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				First Named Inventor		Stephen Melvin Mario D. Nemirovsky	
				Group Art Unit		2154	
				Examiner Name		Larry Donaghue	
Sheet	1	of	2	Attorney Docket Number		MIPS.0167-00-US	
OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS							
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D	AA	DIEFENDORFF, KEITH, "WinChip 4 Thumbs Nose at ILP," <i>Microprocessor Report</i> , Vol. 12, No.16, 10 pages (December 7, 1998)					
S	AB	EGGERS ET AL, "Simultaneous Multithreading: A Platform for Next-Generation Processors", <i>IEEE Micro</i> , 1997.					
D	AC	DIEFENDORFF, KEITH; "Jalapeno Powers Cyrix's M3", <i>Microprocessor Report</i> , Vo. 12, No. 15, Nov. 16, 1998.					
D	AD	BECKER ET AL; "The PowerPC 601 Microprocessor", <i>IEEE Micro</i> , IEEE 1993.					
D	AE	SLATER, MICHAEL, "Rise Joins x86 Fray With mP6" <i>Microprocessor Report</i> , Vol. 12, No. 15, Nov. 16, 1998.					
D	AF	DIEFENDORFF, KEITH; "Compaq Chooses SMT for Alpha", <i>Microprocessor Report</i> , Dec. 6, 1999.					
D	AG	POTEL, M.J., "Real-time Playback in Animation Systems", <i>Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques</i> , 1977, pp.72-77, San Jose, CA.					
D	AH	ARM Architecture Reference Manual, 1996, pp.3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall.					
D	AI	MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp.10-66, 10-67, and 10-71, Motorola, Inc.					
D	AJ	DIFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, <i>IEEE Micro</i> , April 1992, pp.40-63, Vol. 12, No.2.					
D	AK	KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp.7-106 and 7-107, Prentice hall, New Jersey.					
D	AL	DIEFENDORFF, KEITH et al., "Altivec Extension to PowerPC Accelerates Media Processing", March - April 2000, pp.85-95, <i>IEEE Micro</i> , Vol. 20, No.2.					
D	AM	FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp.210-211, <i>IEEE</i> .					
D	AN	YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of CA, Santa Barbara dissertation, December 1995, Santa Barbara, CA.					
D	AO	STEERE et al, "A Feedback-Driven Proportion Allocator for Real Estate Scheduling", <i>Third Symposium on Operating Systems Design and Implementation</i> , February 1999, pp.145-158, USENIX Association.					

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g	AP	YAMAMOTO, WAYNE, et al., "Increasing Superscalar Performance Through Multistreaming", 1995. ✓			
g	AQ	TULLSEN, DEAN, et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22 nd Annual International Symposium on Computer Architecture, June 1995, Santa Margherita, Ligure, Italy. ✓			
g	AR	YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp.42-53. IEEE. ✓			
g	AS	KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of -Order Execution at 600 Mhz", August 1998. ✓			
g	AT	"ESA/390 Principles of Operation" Table of Contents. 09/23/03; http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOKS/DZ9AR001/CCONTENTS .			
g	AU	NEMIROVSKY, MARIO D. et al; "DISC: DYNAMIC INSTRUCTION STREAM COMPUTER", 1191; pp.163-171.			
g	AV	NEMIROVSKY, MARIO D., "DISC, A DYNAMIC INSTRUCTION STREAM COMPUTER", September 1990.			
g	AW	YAMAMOTO, WAYNE et al; "Performance Estimation of Multistreamed, Superscalar Processors", 1994 IEEE, pp. 195-204. ✓			

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